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(54) **HIGH-BANDWIDTH MEMORY APPLICATION WITH CONTROLLED IMPEDANCE LOADING**

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(58) **Field of Classification Search**
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(57) **ABSTRACT**

A microelectronic assembly can include an address bus comprising a plurality of signal conductors each passing sequentially through first, second, third, and fourth connection regions, and first and second microelectronic packages. The first microelectronic package can include first and second microelectronic elements, and the second microelectronic package can include third and fourth microelectronic elements. Each microelectronic element can be electrically coupled to the address bus via the respective connection region. An electrical characteristic between the first and second connection regions can be within a same tolerance of the electrical characteristic between the second and third connection regions.

24 Claims, 6 Drawing Sheets

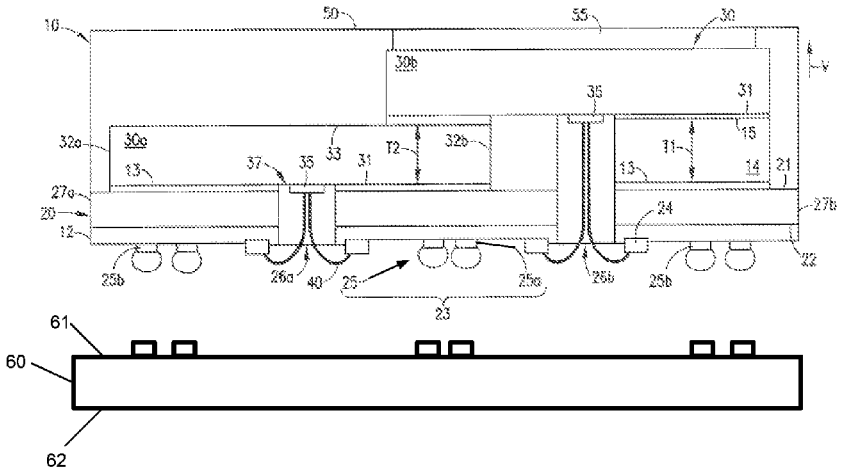

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FIG. 1A

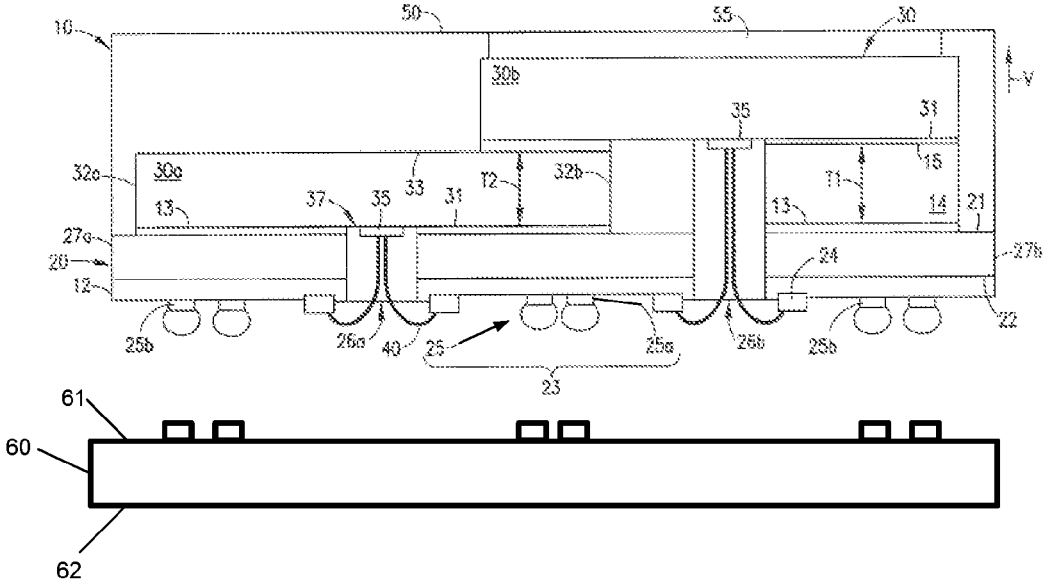
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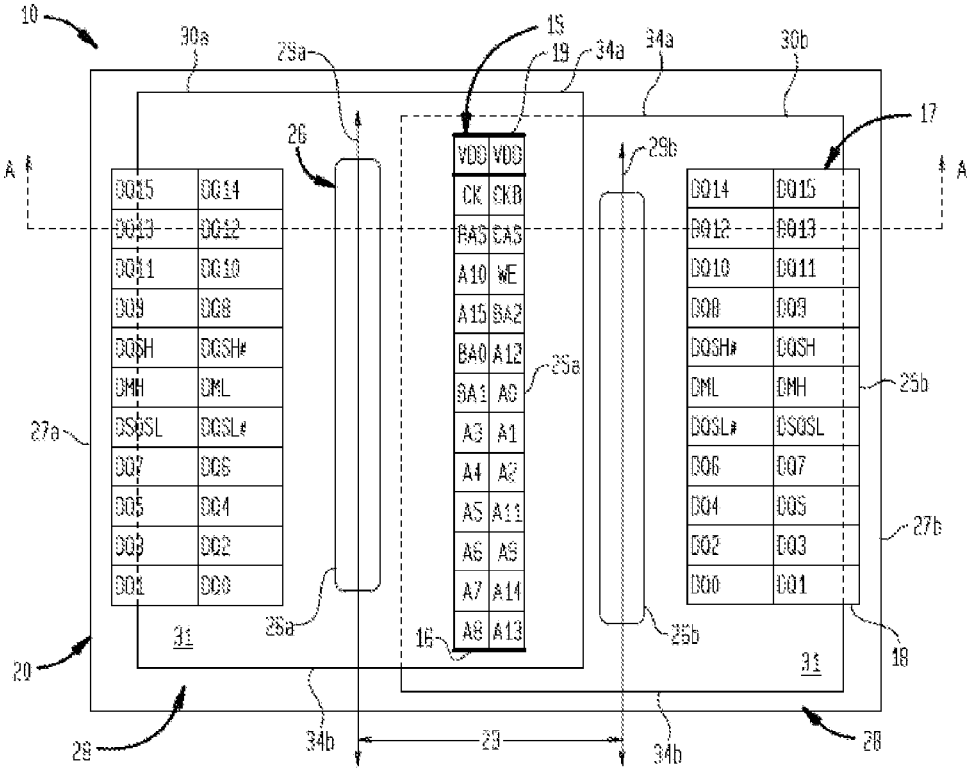
FIG. 1B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DQ10
DQ9
DQ8
DQSH#
DQSH
DML
DMH
DQSL#
DQSL
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
VDD
VDD
CK
CKB
RAS
CAS
A10
WE
A15
BA2
BA0
A12
BA1
A0
A3
A1
A4
A2
A5
A11
A6
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A7
A14
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29
34b

FIG. 1C

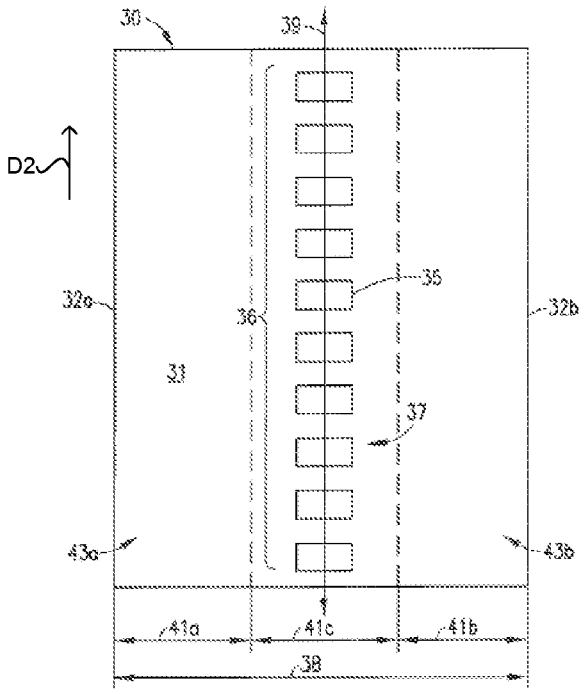


FIG. 1D

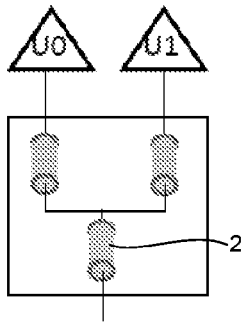


FIG. 2

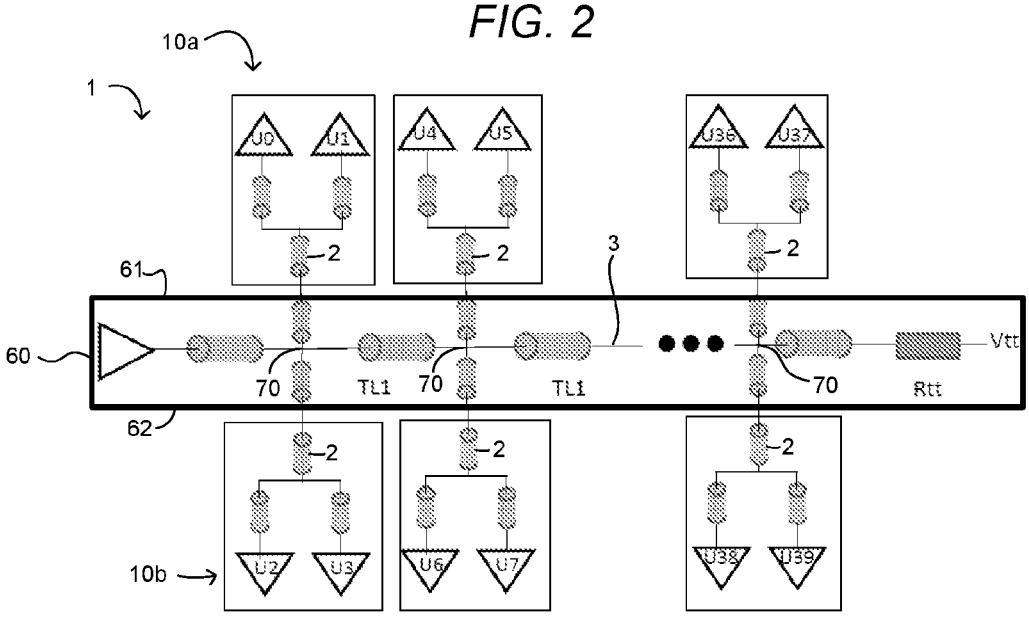


FIG. 3A

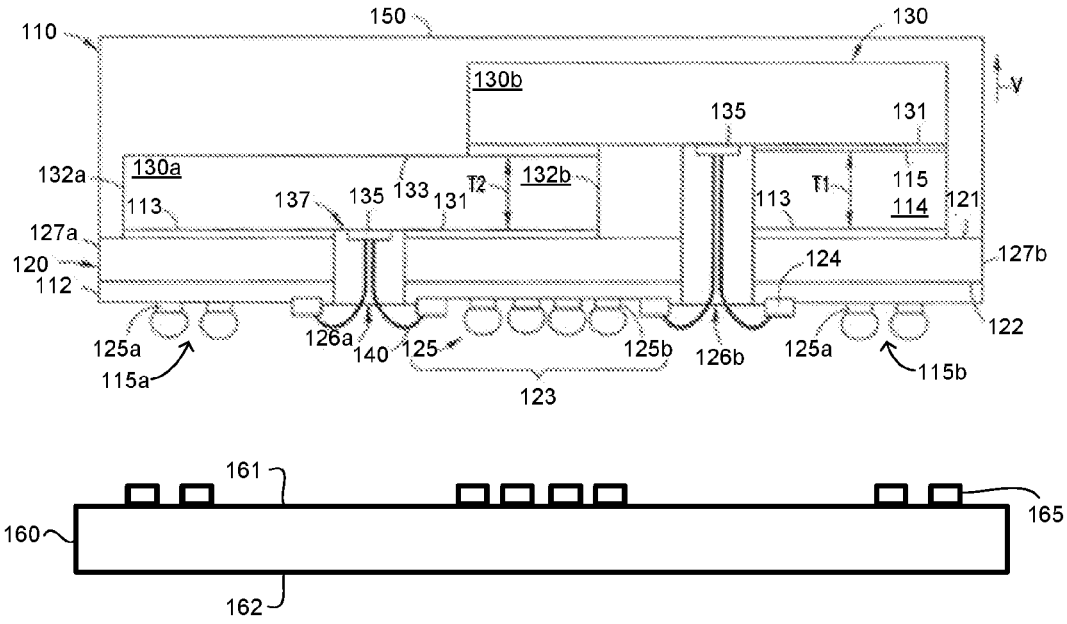


FIG. 3B

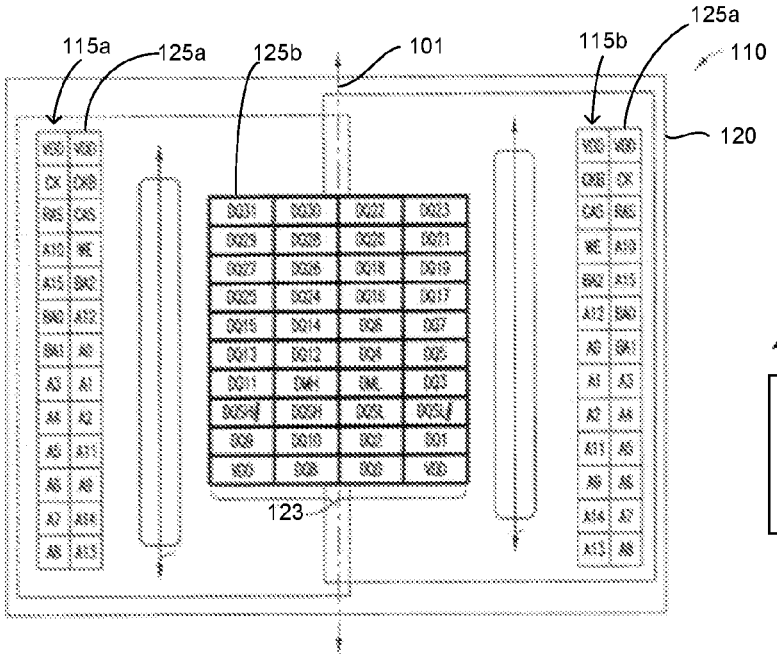
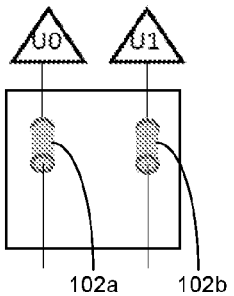


FIG. 3C



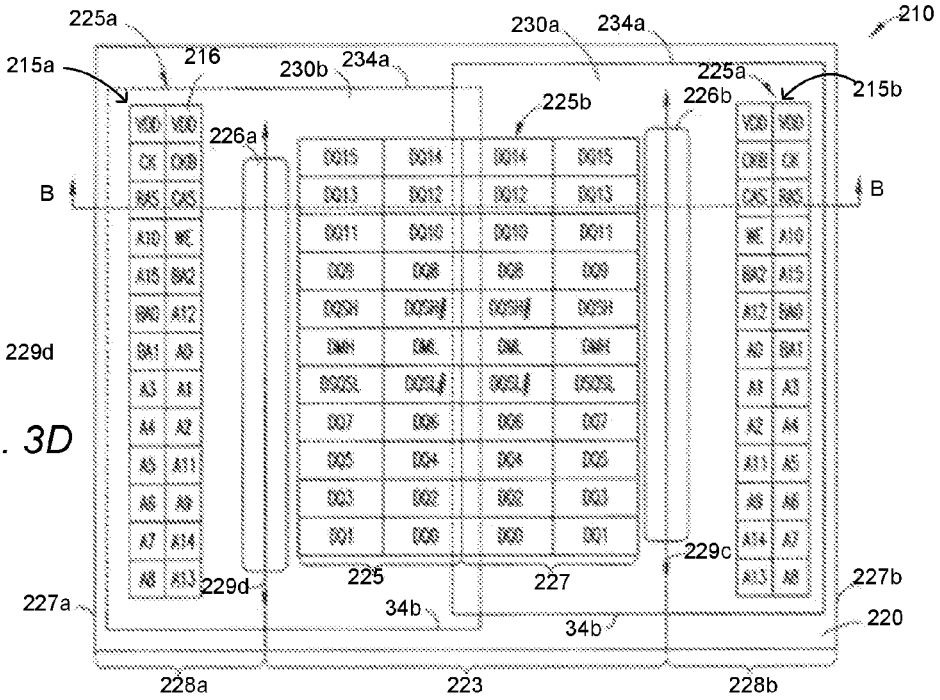


FIG. 3D

FIG. 3E

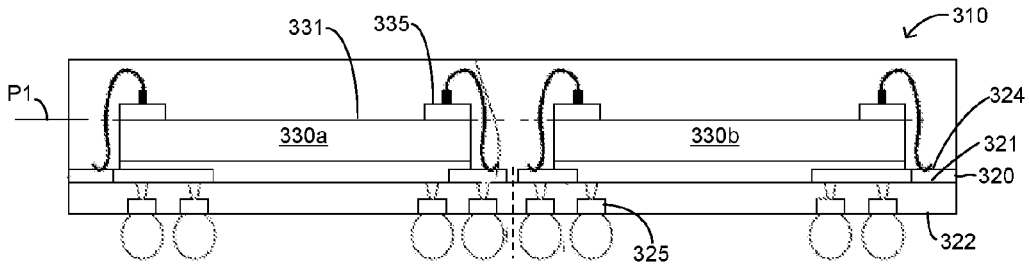


FIG. 3F

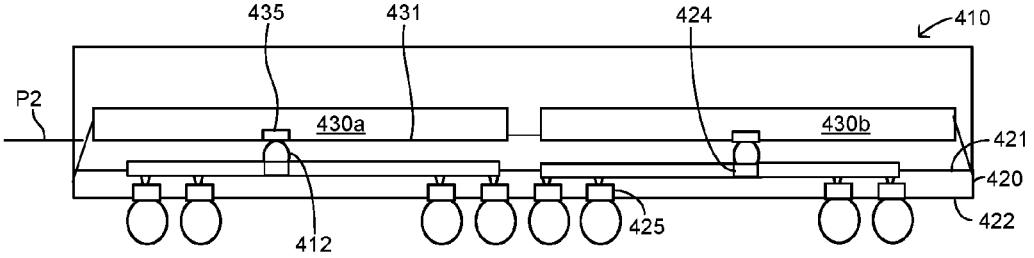


FIG. 3G

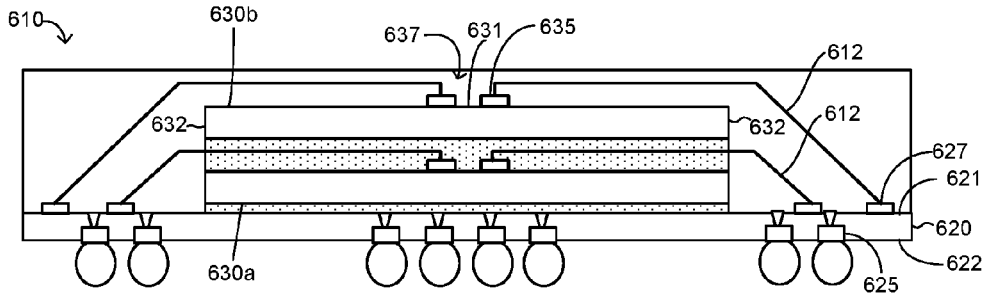


FIG. 3H

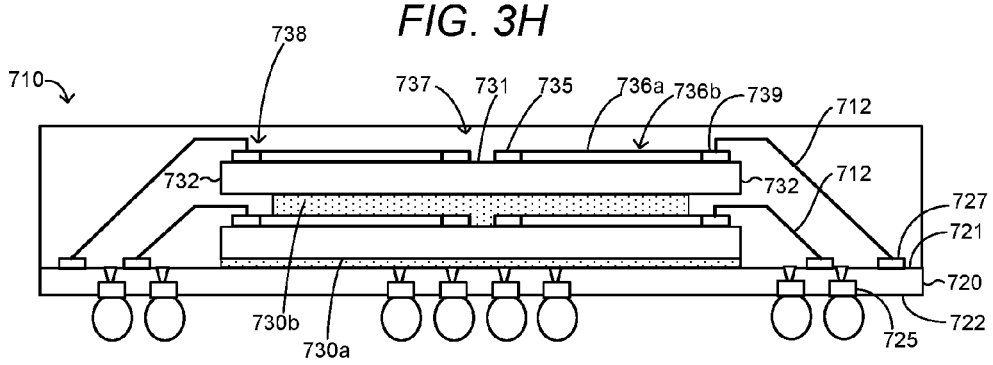
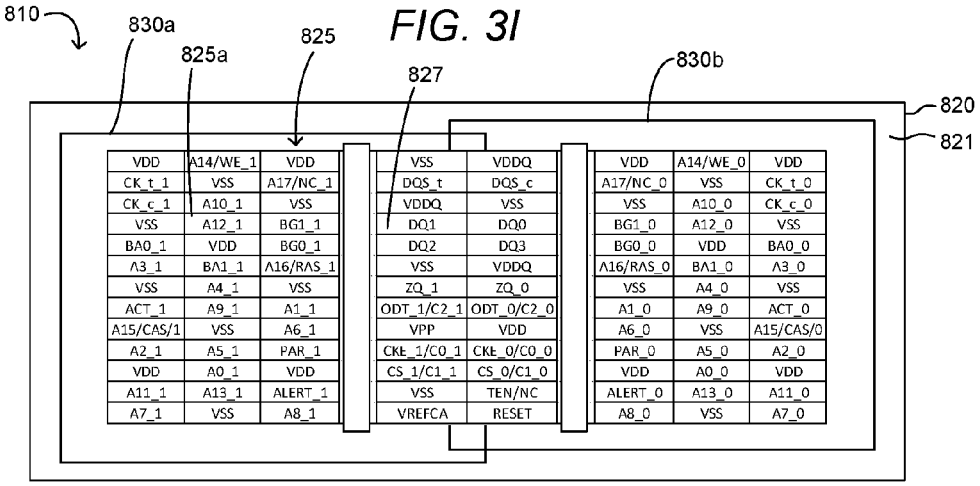


FIG. 3I



VDD	A14/WE_1	VDD	VSS	VDDQ	VDD	A14/WE_0	VDD
CK_t_1	VSS	A17/NC_1	DQS_t	DQS_c	A17/NC_0	VSS	CK_t_0
CK_c_1	A10_1	VSS	VDDQ	VSS	VSS	A10_0	CK_c_0
VSS	A12_1	BG1_1	DQ1	DQ0	BG1_0	A12_0	VSS
BA0_1	VDD	BG0_1	DQ2	DQ3	BG0_0	VDD	BA0_0
A3_1	BA1_1	A16/RAS_1	VSS	VDDQ	A16/RAS_0	BA1_0	A3_0
VSS	A4_1	VSS	ZQ_1	ZQ_0	VSS	A4_0	VSS
ACT_1	A9_1	A1_1	ODT_1/C2_1	ODT_0/C2_0	A1_0	A9_0	ACT_0
A15/CAS/1	VSS	A6_1	VPP	VDD	A6_0	VSS	A15/CAS/0
A2_1	A5_1	PAR_1	CKE_1/C0_1	CKE_0/C0_0	PAR_0	A5_0	A2_0
VDD	A0_1	VDD	CS_1/C1_1	CS_0/C1_0	VDD	A0_0	VDD
A11_1	A13_1	ALERT_1	VSS	TEN/NC	ALERT_0	A13_0	A11_0
A7_1	VSS	A8_1	VREFCA	RESET	A8_0	VSS	A7_0

FIG. 4A

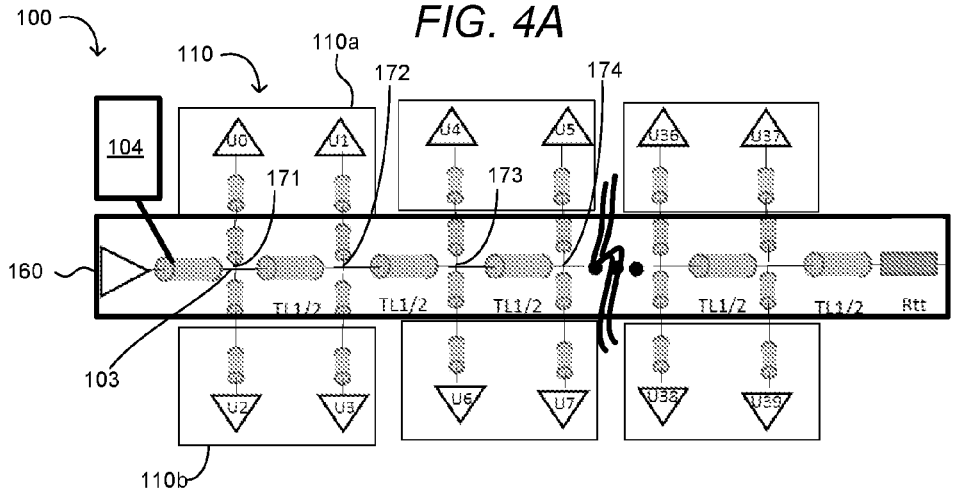


FIG. 4B

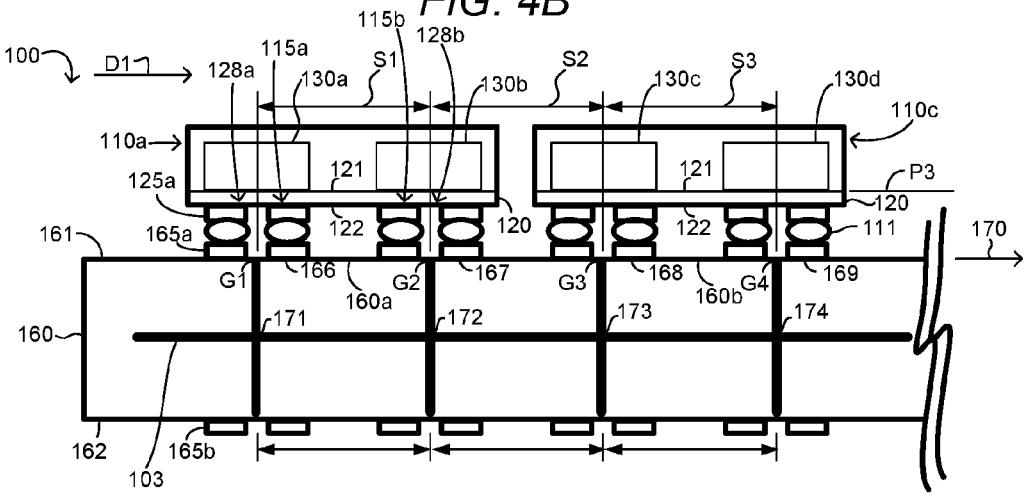
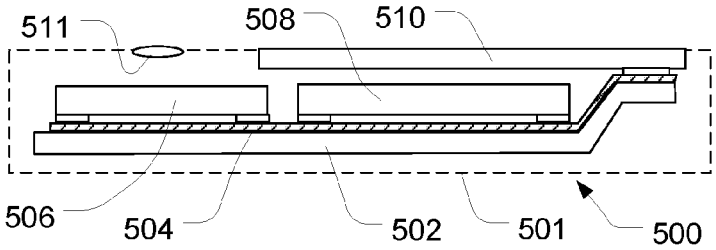


FIG. 5



HIGH-BANDWIDTH MEMORY APPLICATION WITH CONTROLLED IMPEDANCE LOADING

BACKGROUND OF THE INVENTION

The subject matter of the present application relates to microelectronic packages, circuit panels, and microelectronic assemblies incorporating one or more microelectronic package and a circuit panel.

Semiconductor chips are commonly provided as individual, prepackaged units. A standard chip has a flat, rectangular body with a large front face having contacts connected to the internal circuitry of the chip. Each individual chip typically is contained in a package having external terminals connected to the contacts of the chip. In turn, the terminals, i.e., the external connection points of the package, are configured to electrically connect to a circuit panel, such as a printed circuit board. In many conventional designs, the chip package occupies an area of the circuit panel considerably larger than the area of the chip itself. As used in this disclosure with reference to a flat chip having a front face, the "area of the chip" should be understood as referring to the area of the front face.

Size is a significant consideration in any physical arrangement of chips. The demand for more compact physical arrangements of chips has become even more intense with the rapid progress of portable electronic devices. Merely by way of example, devices commonly referred to as "smart phones" integrate the functions of a cellular telephone with powerful data processors, memory, and ancillary devices such as global positioning system receivers, electronic cameras, and local area network connections along with high-resolution displays and associated image processing chips. Such devices can provide capabilities such as full internet connectivity, entertainment including full-resolution video, navigation, electronic banking and more, all in a pocket-size device.

Complex portable devices require packing numerous chips into a small space. Moreover, some of the chips have many input and output connections, commonly referred to as "I/Os." These I/Os must be interconnected with the I/Os of other chips. The components that form the interconnections should not greatly increase the size of the assembly. Similar needs arise in other applications as, for example, in data servers such as those used in internet search engines where increased performance and size reduction are needed.

Semiconductor chips containing memory storage arrays, particularly dynamic random access memory chips (DRAMs) and flash memory chips, are commonly packaged in single- or multiple-chip packages and assemblies. Each package has many electrical connections for carrying signals, power, and ground between terminals and the chips therein. The electrical connections can include different kinds of conductors such as horizontal conductors, e.g., traces, beam leads, etc., that extend in a horizontal direction relative to a contact-bearing surface of a chip, vertical conductors such as vias, which extend in a vertical direction relative to the surface of the chip, and wire bonds that extend in both horizontal and vertical directions relative to the surface of the chip.

Conventional microelectronic packages can incorporate a microelectronic element that is configured to predominantly provide memory storage array function, i.e., a microelectronic element that embodies a greater number of active devices to provide memory storage array function than any other function. The microelectronic element may be or may include a DRAM chip, or a stacked electrically interconnected assembly of such semiconductor chips.

In light of the foregoing, certain improvements in the design of circuit panels or other microelectronic components can be made in order to improve the functional flexibility or electrical performance thereof, particularly in circuit panels or other microelectronic components to which packages can be mounted and electrically interconnected with one another.

BRIEF SUMMARY OF THE INVENTION

A microelectronic assembly can include an address bus comprising a plurality of signal conductors each passing sequentially through first, second, third, and fourth connection regions, and first and second microelectronic packages. The first microelectronic package can include first and second microelectronic elements, and the second microelectronic package can include third and fourth microelectronic elements. Each microelectronic element can be electrically coupled to the address bus via the respective connection region. An electrical characteristic between the first and second connection regions can be within a same tolerance of the electrical characteristic between the second and third connection regions.

In a particular embodiment, the electrical characteristic can be an electrical trace length. In one example, the electrical characteristic can be an electrical propagation delay. In an exemplary embodiment, the electrical characteristic can be a characteristic impedance of the signal conductors. In a particular example, the electrical characteristic can be a difference in an electrical load applied to the address bus from the microelectronic element connected with the respective connection region.

A microelectronic assembly can include an address bus comprising a plurality of signal conductors each passing sequentially through first, second, third, and fourth connection regions, and first and second microelectronic packages. The first microelectronic package can include first and second microelectronic elements, and the second microelectronic package can include third and fourth microelectronic elements. Each microelectronic element can be electrically coupled to the address bus via the respective connection region.

In one embodiment, the microelectronic assembly can also include a controller element electrically coupled to the address bus. The controller element can be configured to control generation of address signals for transmission on the address bus. In a particular example, each of the first, second, third and fourth microelectronic elements can be configured to apply substantially a same load to the address bus as any other of the first, second, third and fourth microelectronic elements. In an exemplary embodiment, characteristic impedances of the signal conductors between the first and second connection regions, and characteristic impedances of the signal conductors between the second and third connection regions can fall within a same tolerance.

In one example, each of the second, third, and fourth connection regions can be configured to receive address signals from the address bus at respective first, second, and third relative delays from the respective first, second, and third connection regions. Any difference among the first, second, and third relative delays can fall within a same tolerance. In a particular embodiment, each of the second, third, and fourth connection regions can have respective first, second, and third relative electrical lengths from the respective first, second, and third connection regions. Any

difference among the first, second, and third relative electrical lengths can fall within a same tolerance.

In one embodiment, each microelectronic element can be electrically coupled to the address bus only at the respective connection region. In a particular example, each microelectronic package can have a substrate, a front surface of each microelectronic element in each microelectronic package can have element contacts thereat, and the front surface of the first and third microelectronic elements can confront a surface of the respective substrate. The front surfaces of the second and fourth microelectronic elements can at least partially overlie a rear surface of the first and third microelectronic elements, respectively. In an exemplary embodiment, each microelectronic package can have a substrate having a surface with substrate contacts thereon.

A front surface of each microelectronic element in each microelectronic package can face away from the surface and can have element contacts thereat coupled with the substrate contacts through electrically conductive structure extending above the front surface. The front surfaces of the microelectronic elements can be arranged in a single plane parallel to the surface. In one example, each microelectronic package can have a substrate. A front surface of each microelectronic element in each microelectronic package can have element contacts thereat and can be arranged in a single plane parallel to a surface of the substrate of the respective microelectronic package. The element contacts of each microelectronic element can face and can be joined to conductive elements at the surface of the substrate of the respective microelectronic package.

In a particular embodiment, each microelectronic element can have memory storage array function. In one embodiment, each microelectronic element can embody a greater number of active devices to provide memory storage array function than any other function. In a particular example, the address bus can be configured to carry all address signals usable by circuitry within the first and second microelectronic packages. In an exemplary embodiment, the address bus can be configured to carry all command signals transferred to each microelectronic package, the command signals being write enable, row address strobe, and column address strobe signals. In one example, wherein the address bus can be configured to carry write enable, row address strobe, and column address strobe signals.

In a particular embodiment, the address bus can be configured to carry all command signals transferred to each microelectronic package, the command signals being write enable, row address strobe, column address strobe, activate, and parity signals. In one embodiment, the address bus can be configured to carry write enable, row address strobe, column address strobe, activate, and parity signals. In a particular example, the microelectronic assembly can also include a circuit panel including the address bus. The first and second microelectronic packages can overlie respective first and second areas of a same surface of the circuit panel.

In an exemplary embodiment, a system can include a microelectronic assembly as described above and one or more other electronic components electrically connected to the microelectronic assembly. In one example, the system can also include a housing. The microelectronic assembly and the one or more other electronic components can be assembled with the housing.

A microelectronic assembly can include a circuit panel comprising a support having an address bus thereon, the address bus comprising a plurality of signal conductors for transmitting address signals, the circuit panel having conductive panel contacts at a surface of the support, the panel contacts being electrically coupled to the signal conductors and comprising first, second, third, and fourth sets of the panel contacts. The microelectronic assembly can also include first and second microelectronic packages each joined to the panel contacts at respective first and second different areas of the surface of the support.

The first package can include first and second microelectronic elements electrically coupled through packaging structure of the first package to the first and second respective sets of panel contacts for receiving the address signals. The second package can include third and fourth microelectronic elements electrically coupled through packaging structure of the second microelectronic package to the third and fourth respective sets of panel contacts for receiving the address signals. Geometric centers of the first, second, and third sets of the panel contacts can have first, second, and third relative separation distances from the geometric centers of the second, third, and fourth sets of the panel contacts, respectively. The first, second, and third relative separation distances can be substantially equal.

In one embodiment, the first and second microelectronic elements can be electrically coupled to the first and second respective sets of panel contacts through first and second respective sets of terminals of the first package, and the third and fourth microelectronic elements can be electrically coupled to the third and fourth respective sets of panel contacts through respective third and fourth sets of terminals of the second microelectronic package. The first and second sets of terminals can be disposed in respective first and second opposite peripheral regions of the first package, and the third and fourth sets of terminals can be disposed in respective third and fourth opposite peripheral regions of the second package.

In a particular example, each peripheral region can occupy a peripheral one-third of a width of a surface of the respective package that faces the surface of the support. In an exemplary embodiment, the terminals can be configured to carry all of the address signals usable by circuitry within the first and second microelectronic packages. In one example, each of the sets of the terminals can be configured to carry all of the same address signals. In a particular embodiment, signal assignments of corresponding ones of the terminals in the first and second sets can be symmetric about a theoretical axis between the first and second sets. In one embodiment, signal assignments of corresponding ones of the terminals in the first and second sets may not be symmetric about a theoretical axis between the first and second sets.

A system can include a support having an address bus thereon comprising a plurality of signal conductors, and first, second, third and fourth sets of conductive contacts at a surface of the support electrically coupled to the signal conductors. Geometric centers of the sets of contacts can be equally spaced from one another along a common theoretical axis. The system can also include a microelectronic package comprising first and second microelectronic elements. At least a first one of the sets of contacts can be electrically coupled to the first microelectronic element. At least a second one of the sets of contacts can be coupled to the second microelectronic element.

In one embodiment, the first microelectronic element can have address inputs coupled only to the first set of contacts, and the second microelectronic element can have address inputs coupled only to the second set of contacts. In a particular example, each microelectronic element can embody a greater number of active devices to provide memory storage array function than any other function. In an

exemplary embodiment, each of the sets of contacts can be configured to carry address information usable by circuitry within the microelectronic packages and command signals transferred to the microelectronic packages. The command signals can include write enable, row address strobe, and column address strobe signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a sectional view of a microelectronic assembly including a microelectronic package and a circuit panel according to an embodiment of the present invention.

FIG. **1**B is a diagrammatic plan view of the microelectronic package shown in FIG. **1**A.

FIG. **1**C is a diagrammatic plan view of one of the microelectronic elements shown in FIG. **1**A.

FIG. **1**D is a diagrammatic representation of the electrical connections for address signals within the microelectronic package shown in FIG. **1**A.

FIG. **2** is a diagrammatic representation of the electrical connections for address signals within a microelectronic assembly including the microelectronic package shown in FIG. **1**A.

FIG. **3**A is a sectional view of a microelectronic assembly including a microelectronic package and a circuit panel according to another embodiment of the present invention.

FIG. **3**B is one potential diagrammatic plan view of the microelectronic package shown in FIG. **3**A.

FIG. **3**C is a diagrammatic representation of the electrical connections for address signals within the microelectronic package shown in FIG. **1**A.

FIG. **3**D is another potential diagrammatic plan view of the microelectronic package shown in FIG. **3**A.

FIGS. **3**E-**3**H are sectional views of alternative configurations of microelectronic elements of the microelectronic package shown in FIG. **3**A.

FIG. **3**I is another potential diagrammatic plan view of the microelectronic package shown in FIG. **3**A.

FIG. **4**A is a diagrammatic representation of the electrical connections for address signals within a microelectronic assembly including the microelectronic package shown in FIG. **3**A.

FIG. **4**B is a sectional view a portion of the circuit panel of the microelectronic assembly shown in FIG. **4**B.

FIG. **5** is a schematic depiction of a system according to one embodiment of the invention.

DETAILED DESCRIPTION

FIGS. **1**A and **1**B illustrate a particular type of microelectronic package **10**. As seen in FIGS. **1**A and **1**B, the microelectronic package **10** can include packaging structure, for example, a dielectric element or substrate **20**, e.g., a support element that includes or consists essentially of dielectric material, e.g., organic or inorganic dielectric material such as, without limitation, oxides, nitrides, or combinations thereof, epoxies, polyimides, thermoset materials or thermoplastics, or other polymeric materials, or composite materials such as epoxy-glass, which can be FR-4 or BT resin structures, or which can be a portion of a tape utilized in tape-automated bonding ("TAB"), for example. The dielectric element **20** has first and second oppositely facing surfaces **21** and **22**.

In some cases, the dielectric element **20** can consist essentially of a material having a low coefficient of thermal expansion ("CTE") in a plane of the substrate (in a direction parallel to the first surface **21** of the substrate), i.e., a CTE of less than 12 parts per million per degree Celsius (hereinafter, "ppm/° C."), such as a semiconductor material e.g., silicon, or a dielectric material such as ceramic material or silicon dioxide, e.g., glass. Alternatively, the substrate **20** may include a sheet-like substrate that can consist essentially of a polymeric material such as polyimide, epoxy, thermoplastic, thermoset plastic, or other suitable polymeric material or that includes or consists essentially of composite polymeric-inorganic material such as a glass reinforced structure of BT resin (bismaleimide triazine) or epoxy-glass, such as FR-4, among others. In one example, such a substrate **20** can consist essentially of a material having a CTE of less than 30 ppm/° C. in the plane of the dielectric element, i.e., in a direction along its surface.

In FIGS. **1**A and **1**B, the directions parallel to the first surface **21** of the dielectric element **20** are referred to herein as "horizontal" or "lateral" directions, whereas the directions perpendicular to the first surface are referred to herein as upward or downward directions and are also referred to herein as the "vertical" directions. The directions referred to herein are in the frame of reference of the structures referred to. Thus, these directions may lie at any orientation to the normal "up" or "down" directions in a gravitational frame of reference.

A statement that one feature is disposed at a greater height "above a surface" than another feature means that the one feature is at a greater distance in the same orthogonal direction away from the surface than the other feature. Conversely, a statement that one feature is disposed at a lesser height "above a surface" than another feature means that the one feature is at a smaller distance in the same orthogonal direction away from the surface than the other feature.

First and second apertures **26***a*, **26***b* can extend between the first and second surfaces **21**, **22** of the dielectric element **20**. As can be seen in FIG. **1**A, the dielectric element **20** can have two apertures **26***a* and **26***b* extending therethrough. The longest dimensions of the apertures **26***a* and **26***b* can define first and second parallel axes **29***a* and **29***b* (collectively axes **29**). The first and second parallel axes **29***a* and **29***b* can define a central region **23** of the second surface **22** of the dielectric element **20** located between the axes **29***a* and **29***b*. A first peripheral region **28***a* of the second surface is disposed between axis **29***a* and the peripheral edge **27***a* of the dielectric element. A second peripheral region **28***b* of the second surface is disposed between axis **29***b* and a peripheral edge **27***b* of the dielectric element opposite from peripheral edge **27***a*. Hereinafter, a statement that a terminal is disposed between an aperture of a substrate and a given feature of a substrate or package such as a peripheral edge thereof shall mean that the terminal is disposed between an axis of the aperture and the given feature.

The dielectric element **20** can have a plurality of terminals **25**, e.g., conductive pads, lands, or conductive posts at the second surface **22** of the dielectric element **20**. As used in this disclosure with reference to a component, e.g., an interposer, microelectronic element, circuit panel, substrate, etc., a statement that an electrically conductive element is "at" a surface of a component indicates that, when the component is not assembled with any other element, the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to the surface of the component toward the surface of the component from outside the component. Thus, a terminal or other conductive element which is at a surface of a substrate may

project from such surface; may be flush with such surface; or may be recessed relative to such surface in a hole or depression in the substrate.

The terminals **25** can function as endpoints for the connection of the microelectronic package **10** with corresponding electrically conductive elements of an external component such as the contacts of a circuit panel **60**, e.g., printed wiring board, flexible circuit panel, socket, other microelectronic assembly or package, interposer, or passive component assembly, among others. In one example, such a circuit panel can be a motherboard or DIMM module board. In a particular example, the circuit panel **60** can include an element having a CTE less than 30 ppm/° C. In one embodiment, such an element can consist essentially of semiconductor, glass, ceramic or liquid crystal polymer material.

In one example, terminals **25***a* that are disposed in the central region **23** of the second surface **22** of the dielectric element **20** can be configured to carry address signals. These terminals are referred to herein as "first terminals." The first terminals **25***a* comprise terminals configured to carry address information. For example, when the microelectronic elements **30***a*, **30***b* include or are DRAM semiconductor chips, each group of first terminals **25***a* can be configured to carry sufficient address information transferred to the microelectronic package **10** that is usable by circuitry within the package, e.g., row address and column address decoders, and bank selection circuitry of one or more of the microelectronic elements **30** to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within a microelectronic element in the package. In a particular embodiment, the first terminals **25***a* can be configured to carry all the address information used by such circuitry within the microelectronic package **10** to determine an addressable memory location within such memory storage array.

In one example, the first terminals **25***a* can be configured to carry each of a group of signals of a command-address bus of the microelectronic element; i.e., command signals, address signals, bank address signals, and clock signals that are transferred to the microelectronic package, wherein the command signals include write enable, row address strobe, and column address strobe signals, and the clock signals are clocks used for sampling the address signals. While the clock signals can be of various types, in one embodiment, the clock signals carried by these terminals can be one or more pairs of differential clock signals received as differential or true and complement clock signals.

In a particular example in which the microelectronic elements **30***a* and **30***b* include DDR3 type chips, the command signals transferred to the microelectronic elements can include write enable ("WE"), row address strobe ("RAS"), and column address strobe signals ("CAS"). In one example in which the microelectronic elements **30***a* and **30***b* include DDR4 type chips, the command signals transferred to the microelectronic elements can include write enable, row address strobe, column address strobe, activate ("ACT"), and parity ("PAR") signals. Such contacts and/or terminals in packages containing DDR3 or DDR4 chips that are configured to receive the aforementioned command signals can be included in any of the embodiments described herein.

As further seen in FIG. **1**B, in addition to first terminals **25***a*, groups of second terminals **25***b* can be disposed in first peripheral region **28***a* and in second peripheral region **28***b* of the second surface, respectively. In one example, the second terminals **25***b* can be configured to carry one or more of data strobe signals, or other signals or reference potentials such as chip select, reset, power supply voltages, e.g., Vdd, Vddq, and ground, e.g., Vss and Vssq. The second terminals **25***b* may include terminals assigned to carry data signals and also data masks and "on die termination" (ODT) signals used to turn on or off parallel terminations to termination resistors.

Typically, the second terminals are configured to carry all bi-directional data signals for writing of data to and for reading of data from random access addressable locations of at least a main memory storage array within each DRAM microelectronic element. However, in some cases, some of the second terminals can carry uni-directional data signals for input to a microelectronic element for writing of data to a memory storage array, and some of the first terminals can carry uni-directional data signals output from a microelectronic element based on data read from a memory storage array.

The microelectronic package **10** can include joining elements **11** attached to the terminals **25** for connection with an external component. The joining elements **11** can be, for example, masses of a bond metal such as solder, tin, indium, a eutectic composition or combination thereof, or another joining material such as an electrically conductive paste, an electrically conductive adhesive or electrically conductive matrix material or a combination of any or all of such bond metals or electrically conductive materials. In a particular embodiment, the joints between the terminals **25** and contacts of an external component (e.g., the circuit panel **60**) can include an electrically conductive matrix material such as described in commonly owned U.S. patent application Ser. Nos. 13/155,719 and 13/158,797, the disclosures of which are hereby incorporated herein by reference. In a particular embodiment, the joints can have a similar structure or be formed in a manner as described therein.

The microelectronic package **10** can comprise a plurality of microelectronic elements **30** each having a front face **31** facing the first surface **21** of the dielectric element **20**. Although the microelectronic elements **30** are shown in FIG. **1**A and the other figures as being offset from one another in a direction parallel to the axes **29**, that need not be the case. Such an offset of the microelectronic elements **30** is shown in the figures for improved clarity of the overlying location of the microelectronic elements with respect to one another. In a particular embodiment, peripheral edges **34***a* of each of the microelectronic elements **30** can lie in a first common plane, and peripheral edges **34***b* opposite the peripheral edges **34***a* of each of the microelectronic elements can lie in a second common plane.

In one example, the microelectronic elements **30** can each comprise a memory storage element such as a dynamic random access memory ("DRAM") storage array or that is configured to predominantly function as a DRAM storage array (e.g., a DRAM integrated circuit chip). As used herein, a "memory storage element" refers to a multiplicity of memory cells arranged in an array, together with circuitry usable to store and retrieve data therefrom, such as for transport of the data over an electrical interface. In one example, each of the microelectronic elements **30** can have memory storage array function. In a particular embodiment, each microelectronic element **30** can embody a greater number of active devices to provide memory storage array function than any other function.

As further seen in FIG. **1**C, each microelectronic element **30** can have a plurality of electrically conductive element contacts **35** exposed at the front surface **31** thereof. The contacts **35** of each microelectronic element **30** can be arranged in one (FIG. **5**C) or in two or more (not shown) columns **36** disposed in a central region **37** of the front face

31 that occupies a central portion of an area of the front face. As used herein with respect to a face (e.g., a front face, a rear face) of a microelectronic element, "central region" means an area, such as region 37, occupying a middle third 41*c* of a distance 38 between opposite peripheral edges 32*a*, 32*b* of the microelectronic element 30 in a direction orthogonal to the edges 32*a*, 32*b*.

The central region 37 is disposed between peripheral regions 43*a*, and 43*b*, each of which lies between the central region 37 and a respective peripheral edge 32*a* or 32*b*, and each peripheral region also occupying an area covering a respective third 41*a* or 41*b* of the distance 38 between the opposite peripheral edges 32*a*, 32*b*. In the particular example shown in FIG. 1C, when the contacts 35 of each microelectronic element 30 are arranged in a central region 37 of the microelectronic element, the contacts can be arranged along an axis 39 that bisects the microelectronic element. As shown in FIG. 1A, the contacts 35 of each microelectronic element 30 can be aligned with at least one of the apertures 26. In one example, the contacts of microelectronic element 30*a* can be aligned only with one of the apertures 26 and the contacts of microelectronic element 30*b* can be aligned only with the other one of the apertures 26.

The microelectronic elements 30 in a microelectronic package 10 can be configured in accordance with one of several different standards, e.g., standards of JEDEC, which specify the type of signaling that semiconductor chips (such as the microelectronic elements 30) transmit and receive through the contacts 35 thereof.

Thus, in one example, each of the microelectronic elements 30 can be of DDRx type, i.e., configured in accordance with one of the JEDEC double data rate DRAM standards DDR3, DDR4, or one or more of their follow-on standards (collectively, "DDRx"). Each DDRx type microelectronic element can be configured to sample the command and address information coupled to the contacts thereof at a first sampling rate, such as once per clock cycle (e.g., on the rising edge of the clock cycle). In particular examples, the DDRx type microelectronic elements can have four, eight or sixteen contacts used for transmitting and receiving bi-directional data signals, each such bi-directional signal referred to as a "DQ" signal. Alternatively, the first terminals of a package can be configured to carry uni-directional data signals such as data signals or "D" signals input to the package and data signals "Q" output from the package, or can be configured to carry a combination of bi-directional and uni-directional data signals.

In another example, each of the microelectronic elements 30 can be of LPDDRx type, i.e., configured in accordance with one of the JEDEC low power double data rate DRAM standards LPDDR3 or one or more of its follow-on standards (collectively, "LPDDRx"). LPDDRx type DRAM chips are available which have 32 contacts assigned to carry DQ signals. There are other differences as well. Each contact 35 on a LPDDRx type DRAM chip may be used to simultaneously carry two different signals in interleaved fashion. For example, each contact 35 on such DRAM chip can be assigned to carry one signal which is sampled on the rising edge of the clock cycle and can also be assigned to carry another signal that is sampled on the falling edge of the clock cycle.

Thus, in LPDDRx type chips, each microelectronic element 30*a*, 30*b* can be configured to sample the command and address information input to the contacts thereof at a second sampling rate, such as twice per clock cycle (e.g., on both the rising edge and on the falling edge of the clock cycle). Accordingly, the number of contacts on the LPDDRx DRAM chip that carry address information or command-address bus information can also be reduced. In a particular example of LPDDRx type chips, one or more of the contacts 35 of each microelectronic element 30*a*, 30*b* can be configured to carry address information at one edge of the clock cycle and command information at another edge of the clock cycle, such that a single contact can be used to alternatingly receive command and address information. Such contacts and/or terminals that are configured to alternatingly receive command and address information can be included in any of the embodiments described herein.

Electrical connections between the contacts 35 and the terminals 25 can include leads, e.g., wire bonds 40, or other possible structure in which at least portions of the leads are aligned with at least one of the apertures 26. For example, as seen in FIG. 1A, at least some of the electrical connections can include a wire bond 40 that extends beyond an edge of an aperture 26 in the dielectric element 20, and is joined at one end to the contact 35 of a microelectronic element and to a conductive element 24 of the dielectric element 20 at another end. In one embodiment, at least some of the electrical connections between the dielectric element and the contacts of the microelectronic element can be through lead bonds, i.e., leads that are integral with other conductive elements on the dielectric element and which extend in a lateral direction along one or both of the first and second surfaces 21, 22 of the dielectric element 20 and are bonded to contacts of one or more of the microelectronic elements, each lead having a portion aligned with at least one of the apertures 26.

In the embodiment of FIGS. 1A-1D, at least some signals that pass through the first terminals 25*a* of the package can be common to at least two of the microelectronic elements 30. These signals can be routed through connections such as conductive traces extending on or within the dielectric element 20 in directions parallel to the first and second surfaces 21, 22 of the dielectric element from the terminals 25 to the corresponding contacts 35 of the microelectronic elements 30. For example, a first terminal 25*a* disposed in the central region 23 of the second surface 22 of the dielectric element 20 can be electrically coupled with a conductive contact 35 of each microelectronic element 30 through a conductive trace, a conductive element 24, e.g., a bond pad, and a wire bond 40 joined to the conductive element 24 and the contact 35.

Referring again to FIG. 1A, a spacer 14 can be positioned between the front surface 31 of the second microelectronic element 30*b* and a portion of the first surface 21 of the dielectric element 20. Such a spacer 14 can be made, for example, from a dielectric material such as silicon dioxide, a semiconductor material such as silicon, and may include one or more layers 13, 15 of adhesive. In one embodiment, the spacer 14 can have substantially the same thickness T1 in a vertical direction V substantially perpendicular to the first surface 21 of the dielectric element 20 as the thickness T2 of the first microelectronic element 30*a* between the front and rear surfaces 31, 33 thereof. In addition, the one or more adhesive layers 13, 15 can be positioned between the first microelectronic element 30*a* and the dielectric element 20, between the first and second microelectronic elements 30*a* and 30*b*, between the second microelectronic element 30*b* and the spacer 14, and between the spacer 14 and the dielectric element 20.

The microelectronic package 10 can also include an encapsulant 50 that can optionally cover, partially cover, or leave uncovered the rear surfaces 33 of the microelectronic elements 30. For example, in the microelectronic package 10

shown in FIG. **1**A, an encapsulant can be flowed, stenciled, screened or dispensed onto the rear surfaces **33** of the microelectronic elements **30**. The microelectronic package **10** can further include an encapsulant (not shown) that can optionally cover the wire bonds **40** and the conductive elements **24** of the dielectric element **20**. Such an encapsulant can also optionally extend into the apertures **26**, and it can cover the contacts **35** of the microelectronic elements **30**.

As can be seen in FIG. **1**D, each of the memory arrays U**0**, U**1** of the microelectronic package **10** can have a shared electrical connection **2** to the set of first terminals **25***a* on the microelectronic package.

Referring to FIG. **2**, in accordance with an aspect of the invention, a microelectronic assembly **1** can include first and second microelectronic packages **10***a*, **10***b* assembled with a circuit panel **60** in a clamshell arrangement. Specifically, as seen in FIG. **2**, the packages **10***a*, **10***b* can be mounted opposite one another to respective panel contacts at first and second surfaces **61**, **62** of a circuit panel **60**, such that the first package **10***a* occupies the same or substantially the same area of the circuit panel as the second package **10***b*.

Each of the microelectronic packages **10** of the microelectronic assembly **1** can have a similar structure that includes first and second microelectronic elements **30** as described above. As can be seen in FIG. **2**, each of the memory arrays U**0** through U**39** of the microelectronic elements **30** within the microelectronic packages **10** can have a shared electrical connection **2** to a connection region **70** of an address bus or command/address bus **3** on the circuit panel **60**.

FIGS. **3**A and **3**B illustrate a microelectronic package **110** that is a variation of the microelectronic package **10** of FIGS. **1**A and **1**B. Each feature or element of the microelectronic package **110** can be the same as a corresponding feature or element of the microelectronic package **10**, except as otherwise described below.

As seen in FIGS. **3**A and **3**B, the microelectronic package **110** can include packaging structure, for example, a dielectric element or substrate **120**. The dielectric element **120** has first and second oppositely facing surfaces **121** and **122**. The longest dimensions of the apertures **126***a* and **126***b* can define first and second parallel axes **129***a* and **129***b*. The first and second parallel axes **129***a* and **129***b* can define a central region **123** of the second surface **122** of the dielectric element **120** located between the axes **129***a* and **129***b*. The second surface **122** has a first peripheral region **128***a* between axis **129***a* and the peripheral edge **127***a* of the dielectric element **120**, and a second peripheral region **128***b* between axis **129***b* and the peripheral edge **127***b* of the dielectric element.

The microelectronic package **110** can include joining elements **111** attached to the terminals **125** for connection with an external component. The microelectronic package **110** can comprise a plurality of microelectronic elements **130** each having a front face **131** facing the first surface **121** of the dielectric element **120**. As further seen in FIG. **3**A, each microelectronic element **130** can have a plurality of electrically conductive element contacts **135** exposed at the front surface **131** thereof. Electrical connections between the contacts **135** and the terminals **125** can include leads, e.g., wire bonds **140**, or other possible structure in which at least portions of the leads are aligned with at least one of the apertures **126**.

As further seen in FIG. **3**B, first and second groups **115***a*, **115***b* of first terminals **125***a* can be disposed in the first peripheral region **128***a* and in the second peripheral region **128***b* of the second surface, respectively. Like the first terminals **25***a*, the first terminals **125***a* comprise terminals configured to carry address signals and address information.

In a particular embodiment, the first group **115***a* of first terminals **125***a* can be configured to carry all the address information used by the circuitry within the microelectronic package **10** to determine an addressable memory location within the first microelectronic element **130***a*, and the second group **115***b* of first terminals **125***b* can be configured to carry all the address information used by the circuitry within the microelectronic package **10** to determine an addressable memory location within the second microelectronic element **130***b*. In one example, each group **115***a*, **115***b* of first terminals **125***a* can be configured to carry each of a group of signals of a command-address bus of the corresponding first and second microelectronic element **130***a*, **130***b*; i.e., command signals, address signals, bank address signals, and clock signals that are transferred to the microelectronic package.

In one example, the first group **115***a* of first terminals **125***a* disposed in the first peripheral region **128***a* can have signal assignments that are symmetric about a theoretical axis **101** with the signal assignments of the second group **115***b* of first terminals disposed in the second peripheral region **128***b*. The theoretical axis **101** extends parallel to the longitudinal axis of each of the apertures and is disposed between the proximate edges of the respective apertures. In a particular embodiment, the first group **115***a* of first terminals **125***a* disposed in the first peripheral region **128***a* may have signal assignments that are not symmetric about a theoretical axis **101** with the signal assignments of the second group **115***b* of first terminals disposed in the second peripheral region **128***b*.

Typically, the theoretical axis is disposed at or near the median distance between the proximate edges of the respective apertures. "Symmetric" as used herein in connection with signal assignments of terminals for carrying address information means that the signal assignment of a terminal on a first side of the theoretical axis has a name and numerical weight which are the same as that of another terminal on an opposite side of the axis at a position symmetric about the axis from the terminal on the first side. The "numerical weight" of the address information assigned to a given terminal refers to the place of that address information within the places of an address that is specified by the address information. For example, an address can be specified by 20 address bits A**0** . . . A**19**. Each bit has a numerical weight, from the highest-ordered address information bit A**19**, which has a numerical weight of 19 representing 2^9 (2 to the power of 19), to the lowest-ordered address information bit A**0**, which has a numerical weight of zero representing 2^0 (2 to the power of zero), which is the 1's place of the address.

In a particular embodiment, the first and second groups **115***a*, **115***b* of first terminals **125***a* of the microelectronic package **110** can be configured to have modulo-X symmetry about the theoretical axis **101**. Microelectronic packages having groups of address and/or data terminals having modulo-X symmetry are shown and described in U.S. Pat. Nos. 8,441,111 and 9,123,555, which are hereby incorporated by reference herein in their entireties.

In one example of the microelectronic package **110**, the first group **115***a* of the first terminals **125***a* on a first side of theoretical axis **101** can be electrically coupled with only the first microelectronic element **130***a*, and the second group **115***b* of first terminals on a second side of the theoretical axis can be electrically coupled with only the second microelec-

tronic element **130***b*. In a particular example, the first group **115***a* of first terminals **125***a* can be electrically coupled with a first rank or first channel of memory access in the microelectronic package **110**, and the second group **115***b* of first terminals can be electrically coupled with a second rank or second channel of memory access in the microelectronic package.

In one example, second terminals **125***b* that are disposed in the central region **123** of the second surface **122** of the dielectric element **120** can be configured to carry one or more of data strobe signals, or other signals or reference potentials such as chip select, reset, power supply voltages, e.g., Vdd, Vddq, and ground, e.g., Vss and Vssq. The second terminals **125***b* may include terminals assigned to carry data signals and also data masks and "on die termination" (ODT) signals used to turn on or off parallel terminations to termination resistors.

In the embodiment of FIG. **3**B, at least some signals that pass through the second terminals **125***b* of the package can be common to at least two of the microelectronic elements **130**. For example, a second terminal **125***a* disposed in the central region **123** of the second surface **122** of the dielectric element **120** can be electrically coupled with a conductive contact **135** of each microelectronic element **130** through a conductive trace, a conductive element **124**, e.g., a bond pad, and a wire bond **140** joined to the conductive element **124** and the contact **135**.

In the particular example of FIG. **3**B, memory storage arrays of the first and second microelectronic elements **130***a*, **130***b* can collectively function to provide access to two relatively wide ranks of memory. For example, a single package **110** can provide two ranks of 32 bit memory access in which 32 second terminals **125***b* on the package **110** can be coupled with 32 DQ contacts of the first microelectronic element **130***a* and can be assigned to carry 32 bi-directional data signals DQ**0** . . . DQ**31**, and can also be coupled with 32 DQ contacts of the second microelectronic element **130***b*.

In an alternative to the terminal configuration of the microelectronic package **110** described above, FIG. **3**D shows a microelectronic package **210** that has two groups **225**, **227** of second terminals, each group of which includes 16 DQ terminals electrically coupled to 16 DQ contacts of one or more of the microelectronic elements **230***a*, **230***b* included in the microelectronic package **210**.

In the particular example of FIG. **3**D, memory storage arrays of the first and second microelectronic elements **130***a*, **130***b* can collectively function to provide access to a single relatively wide rank of memory. For example, a single package **110** can provide a single rank of 32 bit memory access in which 16 DQ contacts of the first microelectronic element **130***a* are coupled to a first group **123** of the DQ terminals **125***b* on the package assigned to carry sixteen bi-directional data signals DQ**0** . . . DQ**15**, and 16 DQ contacts of the second microelectronic element **130***b* are coupled to a second, different group **127** of the DQ terminals **25***a* on the package which are assigned to carry sixteen other bi-directional data signals DQ**0** . . . DQ**15**. In this case, thirty-two bi-directional data signals are transferred in tandem on the thirty-two DQ terminals to support the 32 bit single rank memory access. Specifically, 32 bi-directional data signals are received simultaneously, i.e., on the same clock cycle by said first and second microelectronic elements through said 32 DQ terminals and 32 bi-directional data signals are output simultaneously, on the same clock cycle, by said first and second microelectronic elements through said 32 DQ terminals.

As can be seen in FIG. **3**C, each of the memory arrays U**0**, U**1** of the microelectronic package **110** or the microelectronic package **210** can have an independent electrical connection **102***a*, **102***b* to its respective group **115***a*, **115***b* or **215***a*, **215***b* of first terminals **125***a* or **225***a* on the microelectronic package.

Although the microelectronic elements **30** and **130** are shown in FIGS. **1**A and **3**A as being wire bonded to contacts of the substrate with their front faces facing the first surface of the package substrate, that need not be the case. For example, referring to FIG. **3**E, the microelectronic package **310** is a variation of the microelectronic packages **10**, **110**, and **210** described above. The microelectronic package **310** has two microelectronic elements **330***a* and **330***b* each bearing element contacts **335** at a front face **331** thereof, the front faces facing away from the first surface **321** of the substrate **320**. The microelectronic elements **330** are each electrically connected with conductive elements of the substrate **320** by electrically conductive structure such as wire bonds **340** extending above the front face **331** between the element contacts **335** and substrate contacts **324** at the first surface **321** of the substrate. The substrate contacts **324** are electrically connected with the terminals **325** at the second surface **322** of the substrate **320**. As shown in FIG. **3**E, the front faces **331** of the microelectronic elements **330** can be arranged in a single plane P**1** parallel to the first surface **321** of the substrate **320**.

Referring to FIG. **3**F, the microelectronic package **410** is another variation of the microelectronic packages **10**, **110**, **210**, and **310** described above. The microelectronic package **410** has two microelectronic elements **430***a* and **430***b* each bearing element contacts **435** at a front face **431** thereof, the front faces facing toward the first surface **421** of the substrate **420**. The element contacts **435** of the microelectronic elements **430** face and are joined to substrate contacts **424** at the first surface **421** of the substrate **420** by conductive joining material **412** extending therebetween. The substrate contacts **424** are electrically connected with the terminals **425** at the second surface **422** of the substrate **420**. As shown in FIG. **3**F, the front faces **431** of the microelectronic elements **430** can be arranged in a single plane P**2** parallel to the first surface **421** of the substrate **420**.

Referring to FIG. **3**G, the microelectronic package **610** is another variation of the microelectronic packages **10**, **110**, **210**, **310**, and **410** described above. The microelectronic package **610** has two stacked microelectronic elements **630***a* and **630***b* each bearing element contacts **635** at a front face **631** thereof, the front faces facing away from the first surface **621** of the substrate **620**. The element contacts **635** of the microelectronic elements **630** can be electrically coupled to substrate contacts **627** at the first surface **621** of the substrate **620** by electrically conductive structure, for example, film-over-wire bonds **612**, extending therebetween. The substrate contacts **626** can be electrically connected with the terminals **625** at the second surface **622** of the substrate **620**.

As shown in FIG. **3**G, element contacts **635** of the microelectronic elements **630***a* and **630***b* can be disposed in two adjacent parallel columns, and the element contacts can be disposed in a central region **637** of the front face **631** of the respective microelectronic element. As described above with reference to FIG. **1**C, the central region of the front face **631** of the microelectronic elements **630** can occupy a middle third of a distance between opposite peripheral edges **632** of the microelectronic element in a direction orthogonal to the edges.

Referring to FIG. **3**H, the microelectronic package **710** is another variation of the microelectronic packages **10**, **110**, **210**, **310**, **410**, and **610** described above. The microelectronic package **710** has two stacked microelectronic elements **730***a* and **730***b* each bearing element contacts **735** at a front face **731** thereof, the front faces facing away from the first surface **721** of the substrate **720**. The element contacts **735** of the microelectronic elements **730***a* and **730***b* can be disposed in two adjacent parallel columns, and the element contacts can be disposed in a central region **737** of the front face **731** of the respective microelectronic element. The element contacts **735** can be routed by conductive elements **736***a* of a redistribution layer **736***b* to redistribution contacts **739** adjacent the peripheral edges **732** of the front face **731**.

The redistribution contacts **739** of the microelectronic elements **730***a* and **730***b* can be disposed in two parallel columns, and the redistribution contacts can be disposed in peripheral regions **738** of the front face **731** of the respective microelectronic element. The peripheral regions **738** of the front face **731** of the microelectronic elements **730** can each occupy a peripheral third of a distance between opposite peripheral edges **732** of the microelectronic element in a direction orthogonal to the edges. The redistribution contacts **739** can be electrically coupled to substrate contacts **727** at the first surface **721** of the substrate **720** by electrically conductive structure, for example, wire bonds **712**, extending therebetween. The substrate contacts **727** can be electrically connected with the terminals **725** at the second surface **722** of the substrate **720**.

In an alternative to the terminal configuration of the microelectronic packages **110** and **210** described above, FIG. **3**I shows a microelectronic package **810** having a ball map that can apply to the various packages depicted in FIGS. **3**A and **3**E-**3**H. The microelectronic package **810** has an exemplary bailout map of terminals **825** on the first surface **821** of the substrate **820**, wherein terminals A**0**-A**17** are address terminals that can be first terminals **825***a*, and terminals DQ**0**-DQ**3** are data terminals that can be second terminals **825***b*. Other terminals **825** on the bailout map can be as shown in FIG. **3**I. In one example, the microelectronic elements **830***a* and **830***b* in the microelectronic package **810** can be configured in accordance with one of the JEDEC double data rate DRAM standard DDR4.

In another variation of the embodiment of FIGS. **3**A-**3**D, the microelectronic elements **130***a* and **130***b* of FIG. **3**A can be disposed adjacent to one another, with the front faces facing toward the first surface **121** of the substrate **120** and arranged in a single plane parallel to the first surface of the substrate, similar to the side-by-side arrangement of the microelectronic elements **330**, **430** in FIGS. **3**E and **3**F. However, in this variation, similar to the embodiment of FIGS. **3**A-**3**D, each of the microelectronic elements **130***a* and **130***b* can be electrically connected to substrate contacts **124** by leads (e.g., wire bonds **140**) aligned with apertures **126***a*, **126***b* extending through the substrate **120**.

In yet another variation of the embodiments of FIGS. **3**A-**3**I, the substrate can be omitted, such that the microelectronic package **110**, **210**, **310**, or **410** can be in form of microelectronic elements **130**, **230**, **330**, or **430** having packaging structure that includes an electrically conductive redistribution layer overlying the front face **131**, **331**, or **431** of one or both of the microelectronic elements. The redistribution layer has electrically conductive metallized vias extending through a dielectric layer of the package to the element contacts **135**, **335**, or **435** of the microelectronic elements. The redistribution layer may include the terminals **125**, **225**, **325**, or **425** and traces electrically connected with the terminals, such that the terminals are electrically connected with the element contacts, such as through the metallized vias or through metallized vias and electrically conductive traces. In this case, the package can be referred to as a "wafer-level package having a redistribution layer thereon." In an additional variation, such a microelectronic package having a redistribution layer thereon as described above can have one or more columns of the terminals **125**, **225**, **335**, or **435** disposed on areas of the dielectric layer that extend laterally beyond one or more edges of the microelectronic elements. In this case, the package **1410** can be referred to as a "fan-out wafer-level package having a redistribution layer thereon."

Referring to FIG. **4**A, in accordance with an aspect of the invention, a microelectronic assembly **100** can have a plurality of microelectronic packages **110** can assembled with a circuit panel **160** in a clamshell arrangement as shown in FIG. **4**A, or in other arrangements (e.g., only on the first surface **161** of the circuit panel **160**). In the example shown, the microelectronic packages **110** can have a plurality of memory storage arrays U**0** through U**39**, each microelectronic package having two memory storage arrays that are each independently accessible through a corresponding group **115***a* or **115***b* of the first terminals **125***a*.

The microelectronic assembly **100** can include an address bus or command-address bus **103** that can comprise a plurality of signal conductors each passing sequentially through connection regions of the circuit panel **160** such as first, second, third, and fourth connection regions **171**, **172**, **173**, and **174**. The bus **103** can extend within or on a support, which may be a portion of the circuit panel **160**. The bus **103** can comprise a plurality of signal conductors for transmitting address signals or address and command signals. The circuit panel **160** can have conductive panel contacts **165** at a surface of the support, such as the conductive panel contacts **165***a* at the first surface **161** of the circuit panel and the conductive panel contacts **165***b* at the second surface **162** of the circuit panel.

In one example, the address bus **103** can be configured to carry all address signals usable by circuitry within the microelectronic packages **130**. In a particular example (e.g., DDR3 chips), the address bus **103** can be configured to carry all command signals transferred to each of the microelectronic packages **130**, the command signals being write enable, row address strobe, and column address strobe signals. In one embodiment (e.g., DDR4 chips), all of the command signals transferred to each of the microelectronic packages **130** can be write enable, row address strobe, column address strobe, activate, and parity signals. The first terminals **125***a* of each of the microelectronic packages **130** can be configured to carry all of the address signals usable by circuitry within the respective microelectronic package.

As seen in FIG. **4**A, the packages **110***a*, **110***b* can be mounted opposite one another to respective panel contacts at first and second surfaces **161**, **162** of the circuit panel **160**, such that the first package **110***a* occupies the same or substantially the same area of the circuit panel as the package **110***b*. Each of the microelectronic packages can have a similar structure that includes first and second microelectronic elements **130***a*, **130***b* as described above.

On the circuit panel **160**, e.g., a printed circuit board, module card, etc., these above-noted signals of the command-address bus: i.e., command signals, address signals, bank address signals, and clock signals, can be bussed to multiple microelectronic packages **110** that are connected thereto in parallel, particularly to first and second micro-

electronic packages **110***a*, **110***b* mounted to opposite surfaces of the circuit panel in a clamshell configuration.

The circuit panel **160** can have pluralities of electrically conductive first and second panel contacts **165***a* and **165***b* (collectively panel contacts **165**) exposed at the respective first and second surfaces **161**, **162**. The microelectronic packages **110** can be mounted to the panel contacts **165**, for example, by joining elements **111** that can extend between the terminals **125** and the panel contacts.

In one embodiment, the first terminals **125***a* of the respective microelectronic packages **110** functionally and mechanically matched, such that each of first and second groups **115***a* and **115***b* of first terminals can have the same pattern of first terminals **125***a* at the second surface **122** of the dielectric element **120** of the respective microelectronic package **110** with the same function, although the particular dimensions of the length, width, and height of each microelectronic package **110** can be different than that of the other microelectronic packages.

In one example, each of the sets or groups **115***a* and **115***b* of the first terminals **125***a* of each microelectronic package **130** can be configured to carry all of the same address signals. As can be seen in FIG. **4**B, in a particular embodiment, each of the sets or groups **115***a* and **115***b* of the first terminals **125***a* of each microelectronic package **130** can be disposed in respective first and second opposite peripheral regions **128***a*, **128***b* of the second surface **122** of the respective substrate **120**. In one embodiment, each peripheral region **128***a*, **128***b* can occupy a peripheral one-third of a width of the second surface of the respective microelectronic package **130** that faces the first surface **161** of the circuit panel **160**. However, the widths of the peripheral regions **128***a*, **128***b* can be the same or different, and each peripheral region may have the same or a different width than the central region **123**.

The microelectronic assembly **100** can further include a controller package **104** electrically coupled to an address bus or command-address bus **103**. The controller package **104** can include a controller element configured to control generation of address signals for transmission on the bus **103**. In one example, first and second microelectronic packages **110** can overlie respective first and second areas of a same surface of the support or circuit panel **160**, and the controller package **104** can overlie a third area of the circuit panel. Such a controller package **104** may be included in embodiments of the microelectronic assembly **100** where the assembly is a registered DIMM. In other embodiments, the microelectronic assembly may not include the controller package **104** where the assembly is a DIMM without registers, e.g., UDIMM (unregistered DIMM).

As illustrated in FIG. **4**B, signals transported by the address bus or command-address bus **103** can be routed in at least one direction D**1** between connection sites on a circuit panel such as the circuit panel **160** at which a plurality of microelectronic packages **110** are connected, such that signals of the bus reach each connection region **171**, **172**, **173**, **174** at different times.

The at least one direction D**1** can be transverse or orthogonal to a direction D**2** (FIG. **1**C) in which at least one column **136** of a plurality of contacts **135** on at least one microelectronic element **130** extends. In such a way, the signal conductors of the command-address bus **130** on (i.e., on or within) the circuit panel **160** can in some cases be spaced apart from one another in the direction D**2** that is parallel to the at least one column **136** of contacts **135** on a microelectronic element **130** within a microelectronic package **110** connected to, or to be connected to the circuit panel **160**.

In the embodiment shown in FIG. **4**B, the microelectronic packages **110***a* and **110***c* can be first and second microelectronic packages each joined to the panel contacts **165***a* at respective first and second different areas **160***a*, **160***b* of the first surface **161** of the circuit panel **160**. The first microelectronic package **110***a* can include first and second microelectronic elements **130***a*, **130***b*, and the second microelectronic package **110***c* can include third and fourth microelectronic elements **130***c*, **130***d*.

The first terminals **125***a* of the microelectronic packages **110***a* and **110***c* can be electrically coupled to first, second, third, and fourth sets **166**, **167**, **168**, and **169** of the panel contacts **165***a*. In turn, the first, second, third, and fourth sets **166**, **167**, **168**, and **169** of the panel contacts **165***a* can be electrically coupled to the signal conductors of the bus **103**. In one example (e.g., DDR3 chips), each of the sets **166**, **1167**, **168**, **169** of panel contacts **165***a* can be configured to carry address information usable by circuitry within the microelectronic packages **110** and command signals transferred to the microelectronic packages, the command signals being write enable, row address strobe, and column address strobe signals. In one embodiment (e.g., DDR4 chips), the command signals transferred to the microelectronic packages can be write enable, row address strobe, column address strobe, activate, and parity signals.

Each of the microelectronic elements **130***a*, **130***b*, **130***c*, and **130***d* can be electrically coupled to the signal conductors of the bus **103** at a respective one of the connection regions **171**, **172**, **173**, and **174** via a respective set **166**, **167**, **168**, and **169** of the panel contacts **165***a* and via packaging structure (e.g., first terminals **125***a*) of the respective microelectronic package for receiving address signals or address and command signals.

In the embodiment shown in FIG. **4**B, each of the first, second, third, and fourth microelectronic elements **130***a*, **130***b*, **130***c*, and **130***d* can be electrically coupled to the bus **103** only at the respective one of the first, second, third, and fourth connection regions **171**, **172**, **173**, and **174**. In a particular example, the first microelectronic element **130***a* of a first microelectronic package **110***a* can have address inputs coupled only to the first set **166** of panel contacts **165***a*, and the second microelectronic element **130***b* of the first microelectronic package **110***a* can have address inputs coupled only to the second set **167** of panel contacts **165***a*.

In the example shown in FIG. **4**B, geometric centers G**1**, G**2**, and G**3** of the respective first, second, and third sets **166**, **167**, and **168** of the panel contacts **165***a* have first, second, and third substantially equal relative separation distances S**1**, S**2**, and S**3** from the geometric centers G**2**, G**3**, and G**4** of the second, third, and fourth sets **167**, **168**, and **169** of the panel contacts, respectively. In one example, any difference among the first, second, and third substantially equal relative separation distances S**1**, S**2**, and S**3** can fall within a same tolerance, for example, a same tolerance of ±0.5 mm, or in a particular embodiment, a same tolerance of ±1% of any one of the separation distances.

In one embodiment, the geometric centers G**1**, G**2**, G**3**, and G**4** of the respective first, second, third, and fourth sets **166**, **167**, **168**, and **169** of the panel contacts **165***a* can be equally spaced from one another along a common theoretical axis **170** extending parallel to the first surface **161** of the circuit panel **160**. As used herein, a statement that elements are "equally spaced" with respect one another along a common theoretical axis means that the actual difference in spacing between adjacent ones of the elements is within a typical manufacturing tolerance known to one skilled in the relevant art.

In the embodiment of FIGS. **4**A and **4**B, an electrical characteristic between the first and second connection regions **171**, **172** can be within a same tolerance of the electrical characteristic between the second and third connection regions **172**, **173**. The electrical characteristic can be, for example, an electrical trace length, an electrical propagation delay, a characteristic impedance of the signal conductors, or a difference in electrical load applied to the address bus from the microelectronic element connected with the respective connection region.

In one embodiment, each of the first, second, and third connection regions **171**, **172**, and **173** can have respective first, second, and third relative electrical lengths (i.e., electrical trace lengths) from the respective second, third, and fourth connection regions **172**, **173**, and **174**, and any difference among the first, second, and third relative electrical lengths can fall within a same tolerance, for example, a same tolerance of ±0.5 mm, or in a particular embodiment, a same tolerance of ±1% of any one of the relative electrical lengths. In a particular embodiment, an electrical trace length between the first and second connection regions **171**, **172** can be within a same tolerance of the electrical trace length between the second and third connection regions **172**, **173**.

In a particular embodiment, each of the second, third, and fourth connection regions **172**, **173**, and **174** can be configured to receive address signals from the bus **103** at respective first, second, and third relative delays (i.e., electrical propagation delays) from the respective first, second, and third connection regions **171**, **172**, and **173**, and any difference among the first, second, and third relative delays can fall within a same tolerance, for example, a same tolerance of ±1% of any one of the relative delays. In a particular embodiment, an electrical propagation delay between the first and second connection regions **171**, **172** can be within a same tolerance of the electrical propagation delay between the second and third connection regions **172**, **173**.

In one example, a characteristic impedance of the signal conductors of the bus **103** between the first and second connection regions **171** and **172**, and the characteristic impedance of the signal conductors between the second and third connection regions **172** and **173** can fall within a same tolerance, for example, a same tolerance of ±5 ohms. Likewise, a characteristic impedance of the signal conductors of the bus **103** between the first and second connection regions **171** and **172**, the characteristic impedance of the signal conductors of the bus **103** between the second and third connection regions **172** and **173**, and the characteristic impedance of the signal conductors between the third and fourth connection regions **173** and **174** can fall within a same tolerance, for example, a same tolerance of ±5 ohms.

In one example, each of the first, second, third and fourth microelectronic elements **130***a*, **130***b*, **130***c*, and **130***d* can be configured to apply substantially a same load (i.e., electrical load) to the bus **103** as any other of the first, second, third and fourth microelectronic elements, for example, within a tolerance of ±5 ohms. In a particular embodiment, a difference in electrical load applied to the address bus **103** via the first and second connection regions **171**, **172** can be within a same tolerance of the difference in electrical load applied to the address bus via the second and third connection regions **172**, **173**. For example, the same tolerance of the difference in electrical load applied to the address bus can be within a tolerance of ±5 ohms.

In the examples of the microelectronic assembly **100** described herein having microelectronic packages **110** including microelectronic elements **130** each with independent electrical connections to the address bus or command/address bus **103** (through independent groups **115***a*, **115***b* of first terminals each connected to only one of the microelectronic elements), the electrical loads may be distributed more evenly distributed along the signal conductors of the fly-by bus **103**.

Compared to the microelectronic assembly **1** of FIG. **2**, the structure of the microelectronic assembly **100** may result in better impedance matching between adjacent connection regions along the bus **103**, and more bandwidth capability along the bus to handle higher frequency signals. The inventors have found that in use, compared to the microelectronic assembly **1** of FIG. **2**, the structure of the microelectronic assembly **100** may produce significantly lower reflection, thereby permitting the assembly to operate at a higher bandwidth with better signal transmission.

Although in FIG. **4**B, the microelectronic elements **130** are all shown having their front faces **131** extending within a common plane P**3**, that need not be the case. In a particular example, each of the microelectronic packages **110***a* and **110***c* can have microelectronic elements **130** configured as shown in any of FIGS. **1**A, **3**E, **3**F, or other configurations not shown. For example, in one embodiment, a front surface of each microelectronic element in each microelectronic package can have element contacts thereat, and the front surface of the first and third microelectronic elements **130***a*, **130***c* can confront the first surface **121** of the respective substrate **120**, and the front surfaces of the second and fourth microelectronic elements **130***b*, **130***d* can at least partially overlie a rear surface of the first and third microelectronic elements, respectively.

In one embodiment, the connection regions **171**, **172**, **173**, and **174** need not all be disposed on a single circuit panel. For example, connection regions **171**, **172** to which the microelectronic elements of a first package are coupled can be disposed on a circuit panel other than the circuit panel on which the connection regions **173**, **174** coupled to the second package are disposed.

The microelectronic packages, circuit panels, and microelectronic assemblies described above with reference to FIGS. **1**A through **4**B above can be utilized in construction of diverse electronic systems, such as the system **500** shown in FIG. **5**. For example, the system **500** in accordance with a further embodiment of the invention includes a plurality of modules or components **506** such as the packages, circuit panels, and assemblies as described above, in conjunction with other electronic components **508**, **510** and **511**.

In the exemplary system **500** shown, the system can include a circuit panel, motherboard, or riser panel **502** such as a flexible printed circuit board, and the circuit panel can include numerous conductors **504**, of which only one is depicted in FIG. **5**, interconnecting the modules or components **506**, **508**, **510** with one another. Such a circuit panel **502** can transport signals to and from each of the microelectronic packages and/or microelectronic assemblies included in the system **500**. However, this is merely exemplary; any suitable structure for making electrical connections between the modules or components **506** can be used.

In a particular embodiment, the system **500** can also include a processor such as the semiconductor chip **508**, such that each module or component **506** can be configured to transfer a number N of data bits in parallel in a clock cycle, and the processor can be configured to transfer a number M of data bits in parallel in a clock cycle, M being greater than or equal to N.

In the example depicted in FIG. **5**, the component **508** is a semiconductor chip and component **510** is a display

screen, but any other components can be used in the system **500**. Of course, although only two additional components **508** and **511** are depicted in FIG. **5** for clarity of illustration, the system **500** can include any number of such components.

Modules or components **506** and components **508** and **511** can be mounted in a common housing **501**, schematically depicted in broken lines, and can be electrically interconnected with one another as necessary to form the desired circuit. The housing **501** is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen **510** can be exposed at the surface of the housing. In embodiments where a structure **506** includes a light-sensitive element such as an imaging chip, a lens **511** or other optical device also can be provided for routing light to the structure. Again, the simplified system shown in FIG. **5** is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like can be made using the structures discussed above.

It will be appreciated that the various dependent claims and the features set forth therein can be combined in different ways than presented in the initial claims. It will also be appreciated that the features described in connection with individual embodiments may be shared with others of the described embodiments.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

The invention claimed is:

1. A microelectronic assembly, comprising:

an address bus comprising a plurality of signal conductors each passing sequentially through first, second, third, and fourth connection regions; and

first and second microelectronic packages, the first microelectronic package comprising first and second microelectronic elements and the second microelectronic package comprising third and fourth microelectronic elements, each microelectronic element electrically coupled to the address bus via the respective connection region,

wherein an electrical characteristic between the first and second connection regions is within a same tolerance of the electrical characteristic between the second and third connection regions.

2. The microelectronic assembly as claimed in claim **1**, wherein the electrical characteristic is an electrical trace length.

3. The microelectronic assembly as claimed in claim **1**, wherein the electrical characteristic is an electrical propagation delay.

4. The microelectronic assembly as claimed in claim **1**, wherein the electrical characteristic is a characteristic impedance of the signal conductors.

5. The microelectronic assembly as claimed in claim **1**, wherein the electrical characteristic is a difference in an electrical load applied to the address bus from the microelectronic element connected with the respective connection region.

6. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic element is electrically coupled to the address bus only at the respective connection region.

7. The microelectronic assembly as claimed in claim **1**, further comprising a controller element electrically coupled to the address bus, the controller element configured to control generation of address signals for transmission on the address bus.

8. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic package has a substrate, a front surface of each microelectronic element in each microelectronic package has element contacts thereat, and the front surface of the first and third microelectronic elements confronts a surface of the respective substrate, and the front surfaces of the second and fourth microelectronic elements at least partially overlies a rear surface of the first and third microelectronic elements, respectively.

9. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic package has a substrate having a surface with substrate contacts thereon, a front surface of each microelectronic element in each microelectronic package facing away from the surface and having element contacts thereat coupled with the substrate contacts through electrically conductive structure extending above the front surface, and wherein the front surfaces of the microelectronic elements are arranged in a single plane parallel to the surface.

10. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic package has a substrate, a front surface of each microelectronic element in each microelectronic package has element contacts thereat and is arranged in a single plane parallel to a surface of the substrate of the respective microelectronic package, and the element contacts of each microelectronic element face and are joined to conductive elements at the surface of the substrate of the respective microelectronic package.

11. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic element has memory storage array function.

12. The microelectronic assembly as claimed in claim **1**, wherein each microelectronic element embodies a greater number of active devices to provide memory storage array function than any other function.

13. The microelectronic assembly as claimed in claim **1**, wherein the address bus is configured to carry all address signals usable by circuitry within the first and second microelectronic packages.

14. The microelectronic assembly as claimed in claim **1**, wherein the address bus is configured to write enable, row address strobe, and column address strobe signals.

15. The microelectronic assembly as claimed in claim **1**, further comprising a circuit panel including the address bus, wherein the first and second microelectronic packages overlie respective first and second areas of a same surface of the circuit panel.

16. A system comprising a microelectronic assembly according to claim **1** and one or more other electronic components electrically connected to the microelectronic assembly.

17. The system as claimed in claim **16**, further comprising a housing, the microelectronic assembly and the one or more other electronic components being assembled with the housing.

18. A microelectronic assembly, comprising:

a circuit panel comprising a support having an address bus thereon, the address bus comprising a plurality of signal conductors for transmitting address signals, the circuit panel having conductive panel contacts at a surface of the support, the panel contacts being elec-

trically coupled to the signal conductors and comprising first, second, third, and fourth sets of the panel contacts;

first and second microelectronic packages each joined to the panel contacts at respective first and second different areas of the surface of the support, the first package comprising first and second microelectronic elements electrically coupled through packaging structure of the first package to the first and second respective sets of panel contacts for receiving the address signals, and the second package comprising third and fourth microelectronic elements electrically coupled through packaging structure of the second microelectronic package to the third and fourth respective sets of panel contacts for receiving the address signals,

wherein geometric centers of the first, second, and third sets of the panel contacts have first, second, and third relative separation distances from the geometric centers of the second, third, and fourth sets of the panel contacts, respectively, and the first, second, and third relative separation distances are substantially equal.

19. The microelectronic assembly as claimed in claim **18**, wherein the first and second microelectronic elements are electrically coupled to the first and second respective sets of panel contacts through first and second respective sets of terminals of the first package, and the third and fourth microelectronic elements are electrically coupled to the third and fourth respective sets of panel contacts through respective third and fourth sets of terminals of the second microelectronic package, and

wherein the first and second sets of terminals are disposed in respective first and second opposite peripheral regions of the first package, and the third and fourth sets of terminals are disposed in respective third and fourth opposite peripheral regions of the second package.

20. The microelectronic assembly as claimed in claim **19**, wherein each peripheral region occupies a peripheral one-third of a width of a surface of the respective package that faces the surface of the support.

21. The microelectronic assembly as claimed in claim **18**, wherein the terminals are configured to carry all of the address signals usable by circuitry within the first and second microelectronic packages.

22. The microelectronic assembly as claimed in claim **18**, wherein each of the sets of the terminals is configured to carry all of the same address signals.

23. The microelectronic assembly as claimed in claim **18**, wherein signal assignments of corresponding ones of the terminals in the first and second sets are symmetric about a theoretical axis between the first and second sets.

24. The microelectronic assembly as claimed in claim **18**, wherein signal assignments of corresponding ones of the terminals in the first and second sets are not symmetric about a theoretical axis between the first and second sets.

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